ENCODING CIRCUIT FOR DIGITAL DATA

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Abstract of **JP9246980**

PROBLEM TO BE SOLVED: To turn the operation of an output circuit to an optimum state in a short time by limiting the counted value of the up-down counter of the output circuit to an optional range and limiting the contents of adjustment data corresponding to the counted value.

SOLUTION: A symbol generation circuit 1 respectively bisects the audio data of 16-bit constitution alternately inputted by left and right channels, generates the symbol data(SD) of 8-bit constitution and outputs them in a prescribed order. A parity data(PD) addition circuit 2 rearranges the SD, adds PD and inputs them to an EFM modulation circuit 3 by one frame unit. In the circuit 3, the SD inputted for each frame from the circuit 2 are respectively converted to the encoding data (ED) of 14 bits and inputted to the output circuit 4. The circuit 4 adds the synchronization data of 24 bits and the sub code data of 14 bits to the ED inputted for each frame from the circuit 3, holds the DSV adjustment data of 3 bits between the respective data and outputs them as EFM data.